



Case Studies

高頻交易專用Switch使用案例

Phitech

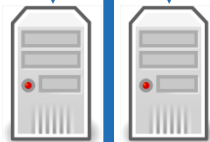
ExaLINK FUSION CASE STUDY 1

Market Data Distribution



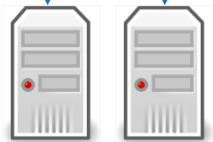
Exchange

Market Data 1對n同時發佈
所有Latency < 5ns



Trading
Systems

- Exchange to Server (sub-5ns)



多台分析系統可同時收到Market Data

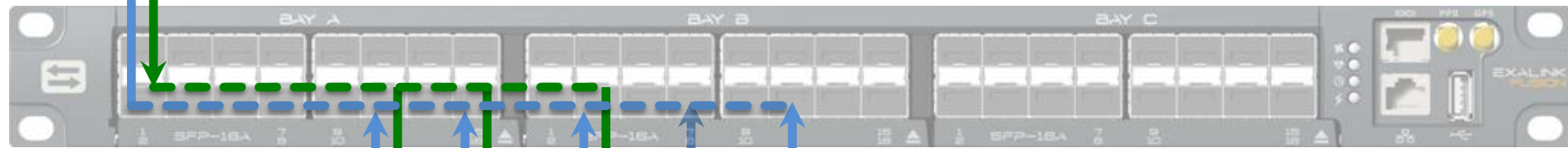
ExaLINK FUSION CASE STUDY 2

Muxing / Aggregation



Exchange

Mux/Aggrgate各交易需求至交易所只要46ns



Trading Systems

- - Exchange to Server(s) (sub-5ns)
- - Server(s) to Exchange (~~55ns~~
46 ns)

ExaLINK FUSION CASE STUDY 3

Electronic Patch Panel / Media Converter



與其它異質
Switch/Router 界接



Primary server

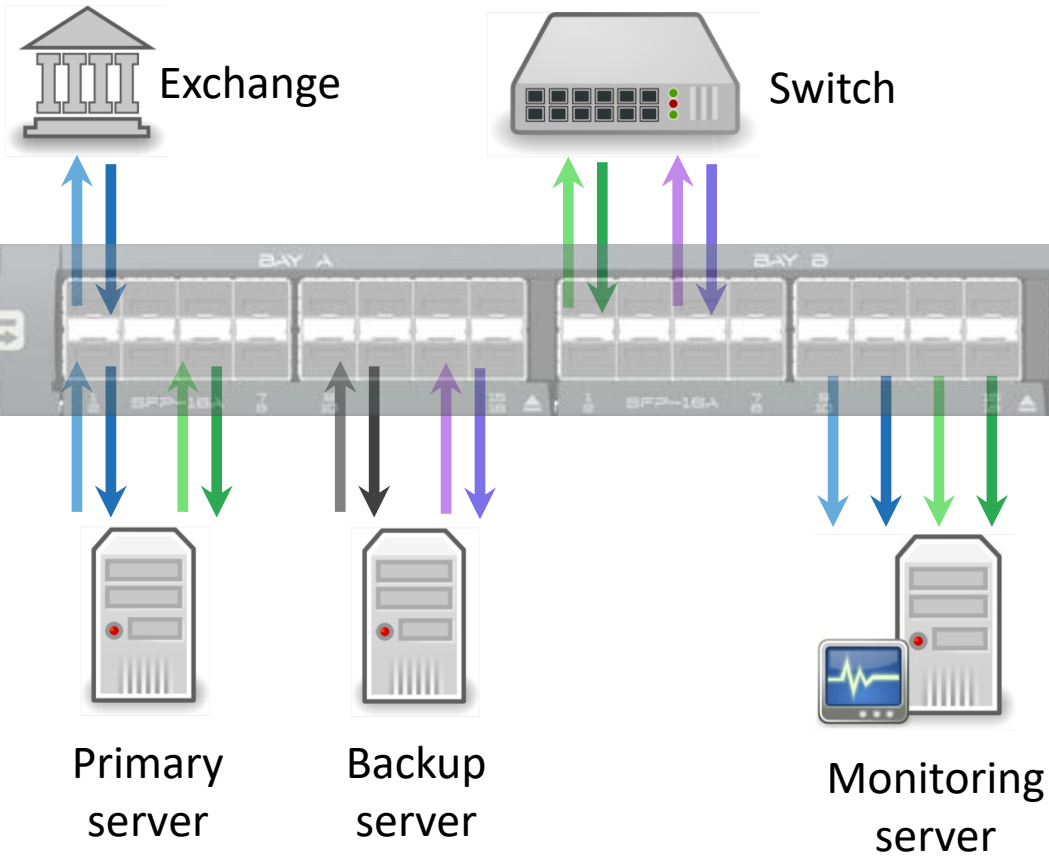


Backup server

- Common use-case which reduces need for remote hands at datacentres and simplifies configuration management
- All connections in the rack made via the ExaLINK FUSION (SFP+ Transceiver)
- Sub 5ns latency = invisible to the network
- Media/Speed conversion 10G / 1G

ExaLINK FUSION CASE STUDY 4

Network monitoring

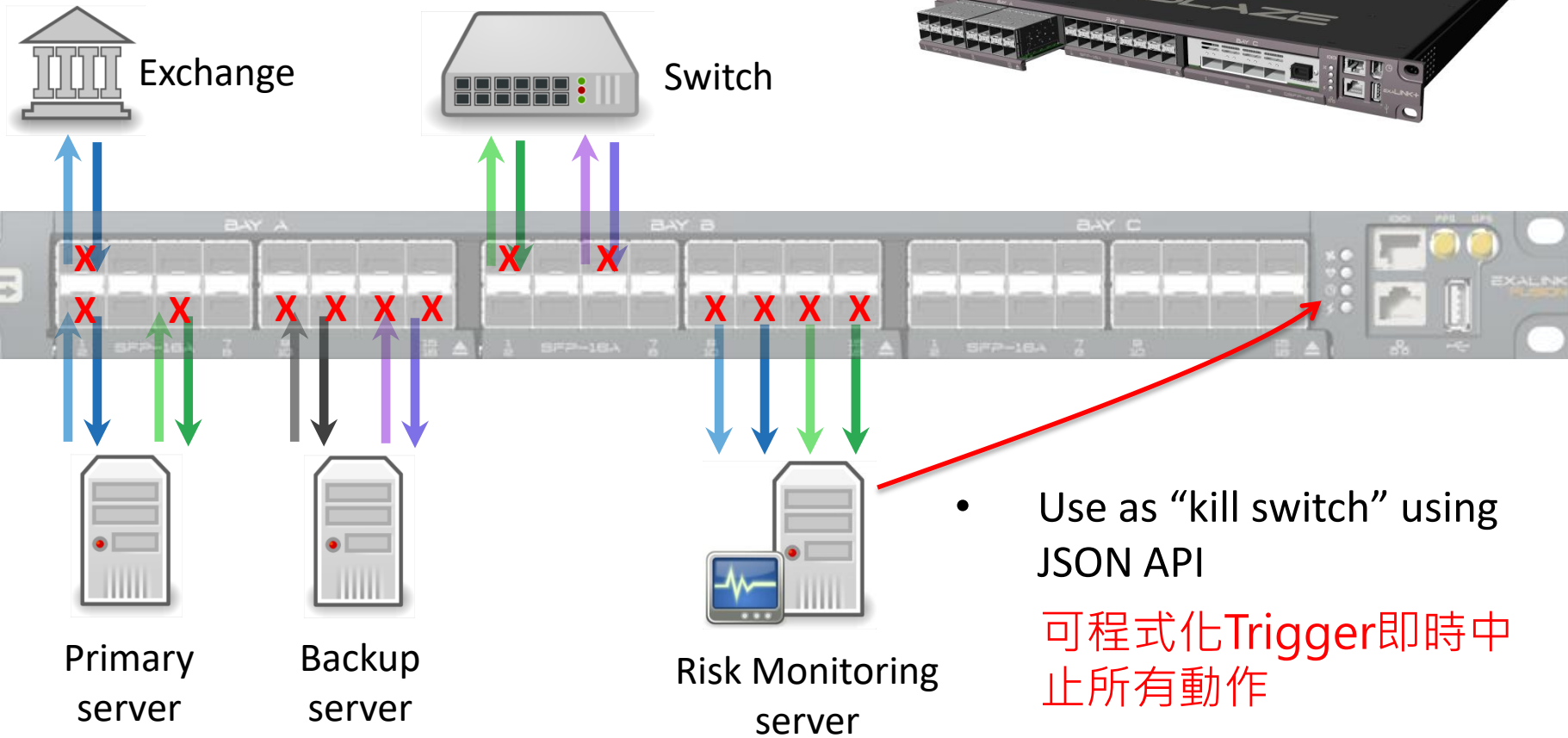


網路流量Tapping後加上
精準Time Stamp, 可作
為網路效能分析來源

- Flexibly sample and monitor a range of ports
- Tapping & Mirroring

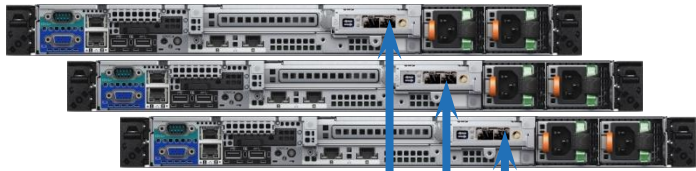
ExaLINK FUSION CASE STUDY 5

Kill Switch / Circuit Breaker



ExaLINK FUSION CASE STUDY 6

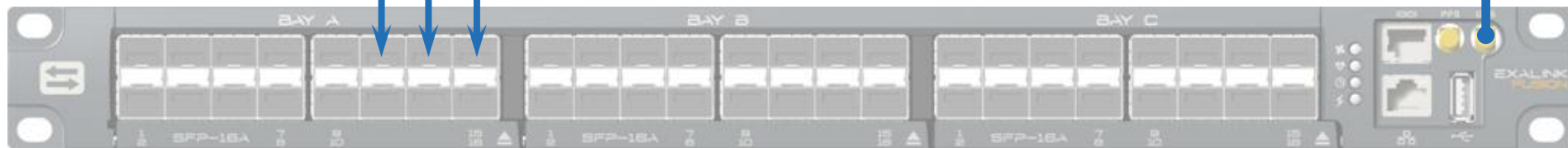
Time Synchronization - PTP



精準校時



GPS antenna



- ExaLINK FUSION used as master
- Normal ExaNIC / Industry standard cards operating as PTP slaves (using hardware time stamping)
- Boundary clock mode on ExaLINK FUSION (future)

ExaLINK FUSION CASE STUDY 7

Time synchronization - PPS



- PPS out from ExaLINK FUSION cascaded through rack
- Tight synchronization achievable (better than PTP)
- Option to transmit time code over PPS port to synchronize actual time of day – coming soon

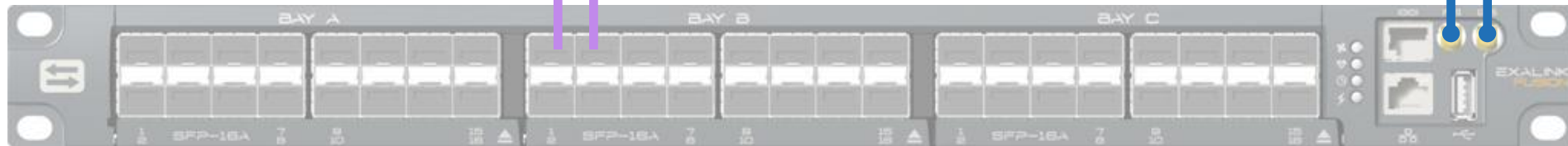
ExaLINK FUSION CASE STUDY 8

Capture & Record (Internal & External)

精準擷取網路封包至外部系統,
Time Stamp可小至2.8ns



GPS antenna



- Using X86 Internal Module for ExaLINK FUSION
- Integrated X40 (8x10G Interfaces with virtual connectivity between Fusion ports and embedded X40 ports)
- X40 can see in/out PPS Fusion port for timing
- Up to 3TB of local storage with line rate recording at 10G
- Patch, Tap, Mirror, Mux, Switch traffic to internal / external record server
- Precision Time Stamping to 2.8ns

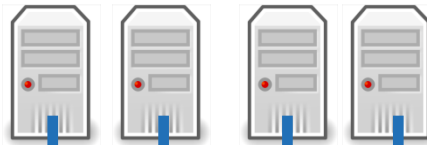
ExaLINK FUSION CASE STUDY 9

Embedded Trading Logic/Risk Server



Exchange

Trading Systems



GPS antenna

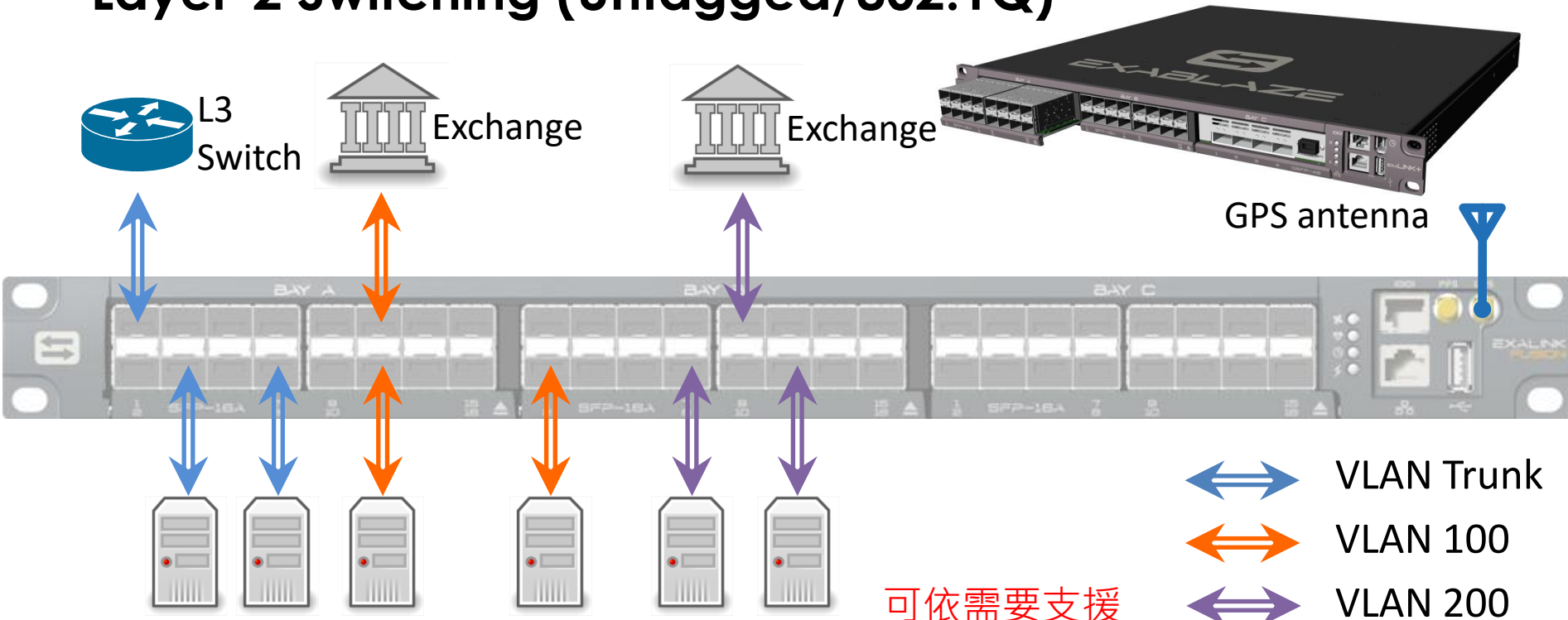


選配內建x86/FPGA模組-可自行開發系統與Switch更緊密結合

- Using X86 Internal Module for ExaLINK FUSION
- Ships with CentOS7 Operating System but not limited to
- Trading Logic / Inline Risk Checks
- Virtual connectivity between Fusion ports and embedded X40 ports
- FPGA DevKit Available for onboard X40
- Intel Active Management Technology Support

ExaLINK FUSION CASE STUDY 10

Layer-2 Switching (Untagged/802.1Q)

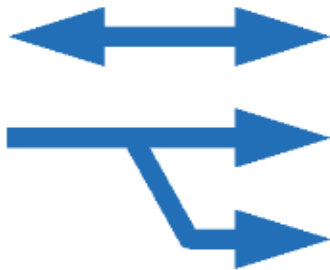


- 可依需要支援
- L1: Tapping
 - L1.5: Mux/Aggregation
 - L2: Switching
- ↔ VLAN Trunk
↔ VLAN 100
↔ VLAN 200



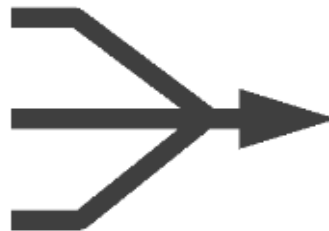
INTRODUCING THE WORLD'S FASTEST LAYER 2+ SWITCH

5 NS FAN-OUT



Patch together any two ports, or fan out multicast data with less than 5 ns latency.

49 NS AGGREGATION



Connect multiple servers to a single uplink port with 49 ns of port to port latency. Everything you need to get to the exchange with nothing you don't.

95 NS LAYER 2+



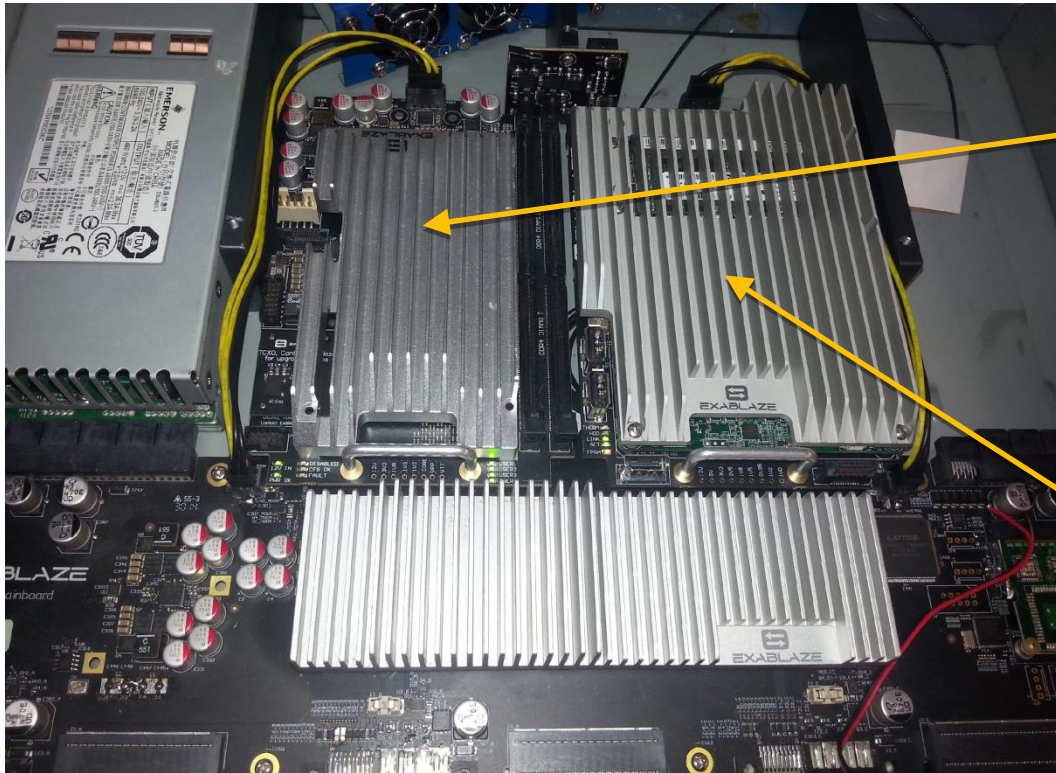
Switch packets at Layer 2 with 95 ns of latency, and a subset of full Layer 3 functionality.

NOW WITH THE FASTEST CROSSPOINT-ENABLED MULTIPLEXER

Aggregate 15 connections to 1 with latency as low as **49 nanoseconds** with [FastMux](#), the world's fastest crosspoint-enabled multiplexer.

附錄1

A POWERFUL COMBINATION...



FPGA Module:

Xilinx Kintex Ultrascale
KU115
288 Mbit QDR4 SRAM
2 x DDR4 DIMM
OCXO, TPM

x86 Module:

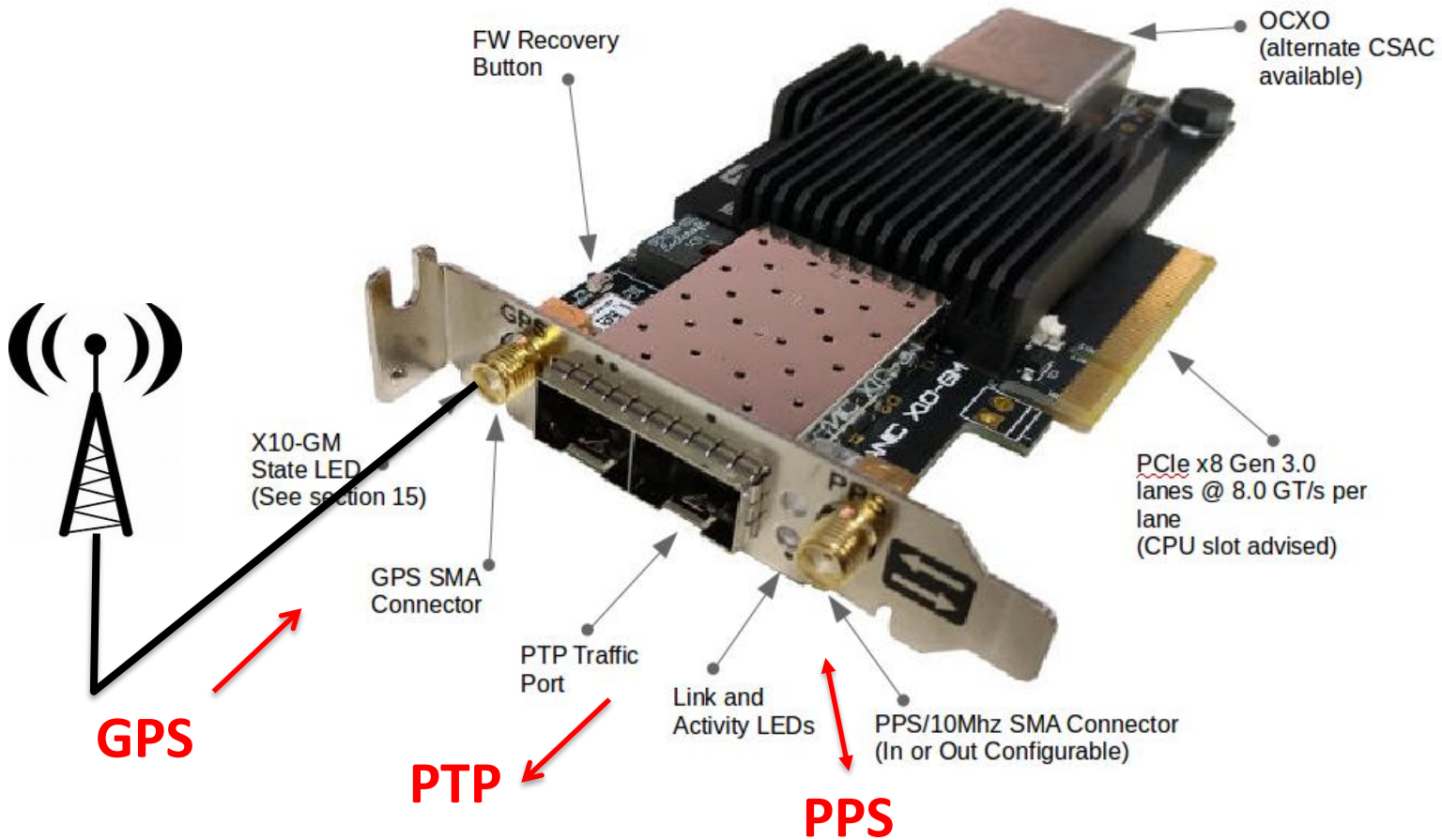
Intel Core-i7 Skylake,
4 cores @ 2.8GHz
32GB DDR4-2133MT/s
Dual mSATA SSDs
M.2 PCIe NVMe SSD
**Onboard low latency
ExaNIC X40**

NICs

- World's Lowest-Latency
- 10GbE, 1GbE, 100M
- Transparent **kernel bypass** - Exasock
- **API** - libexanic
- **Bridging & Mirroring**
- Flow Steering with 32 user space 2MB buffers
 - **128 IP rules per port, 64 MAC rules per port**
- Hardware timestamping
 - All received frames, most recent TX frame
 - Time synch via host, hardware assisted via PTP, optional PPS
- FDK - being used for:
 - **mkt data filtering/tagging. line arbitration**
 - **simple card-based trading strategies**



ExaNIC - Grand Master

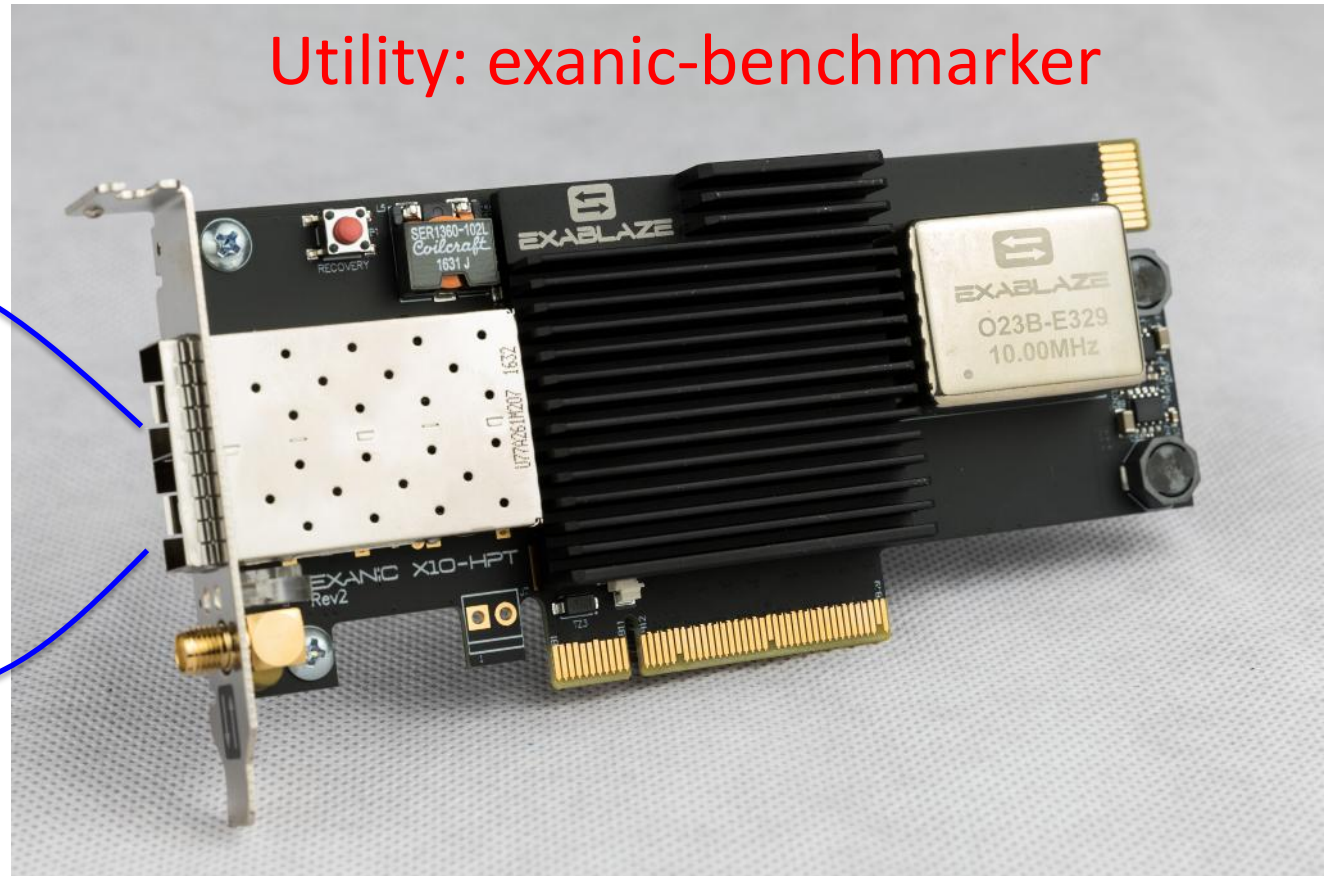


ExaNIC X10 - HPT

Timestamping
0.25 ns

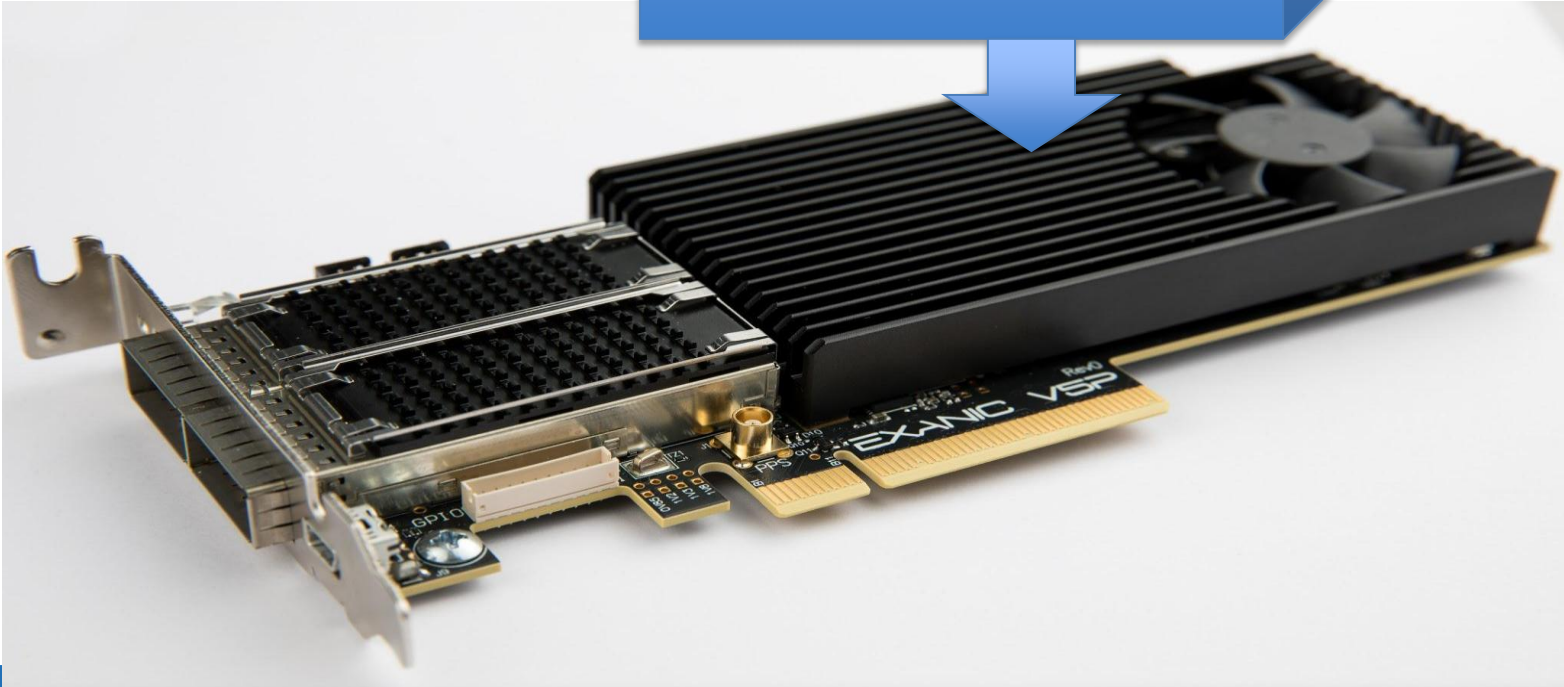
Utility: exanic-benchmarker

Measured Target



ExaNIC V5P

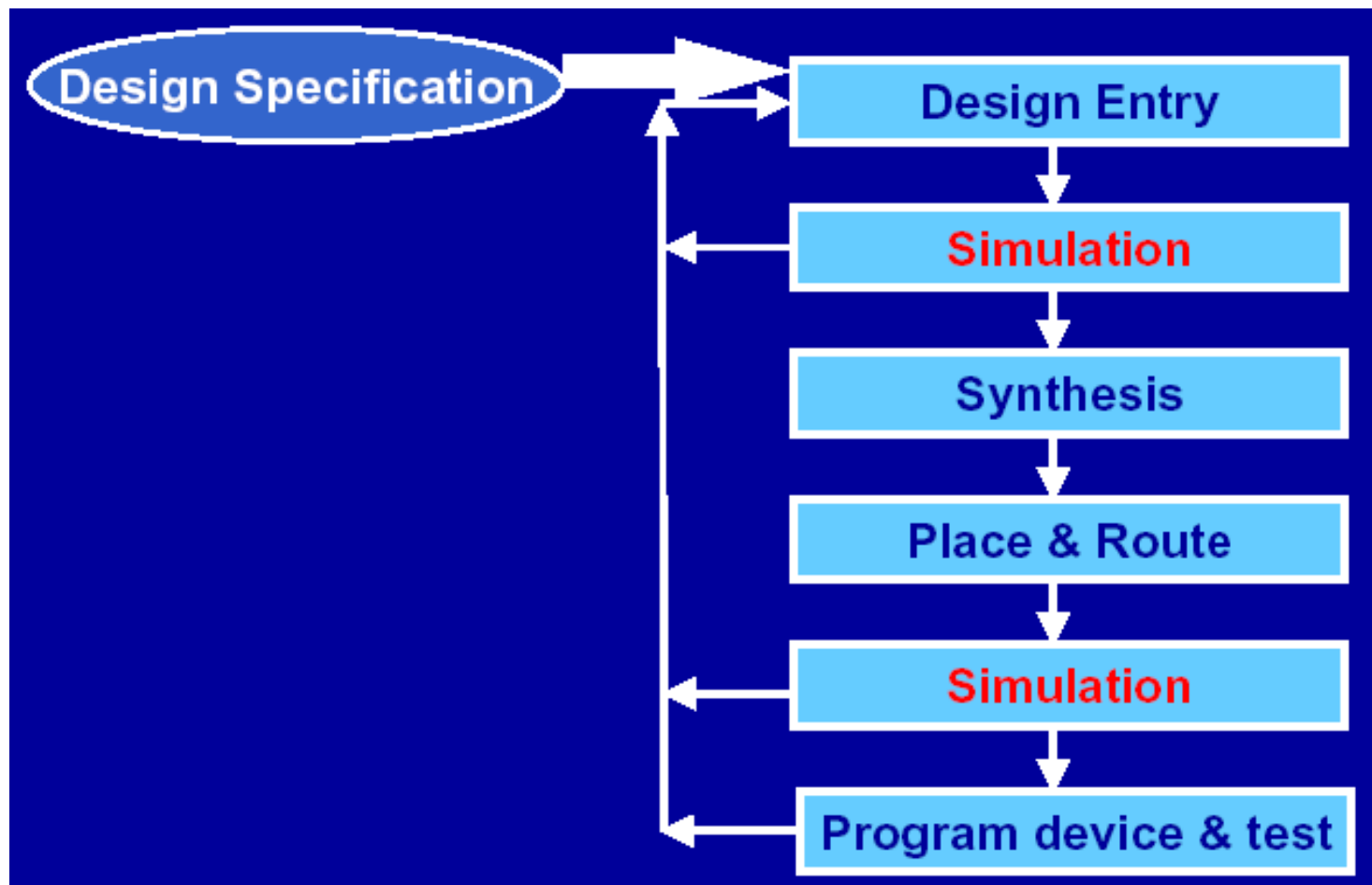
High Density FPGA program



附錄2

FPGA程式開發

FPGA開發流程



FPGA設計與實踐

■ *Xilinx Design Software:*

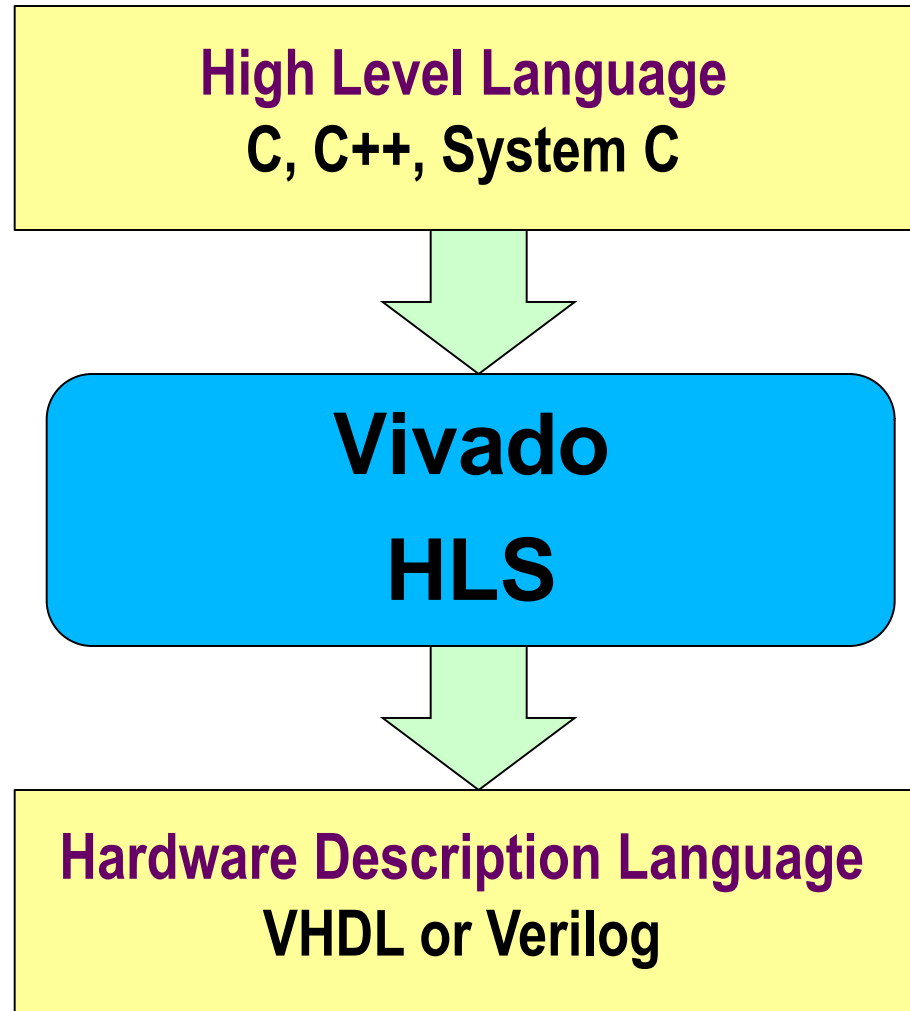
- ✓ Vivado Design Suite (7-Series and newer)
 - ◆ System Edition (in the lab)
 - ◆ WebPACK Edition (free)

■ *FPGA boards:*

- ✓ On ExaNIC Network Adaptor
- ✓ On Module inside ExaLINK FUSION Switch

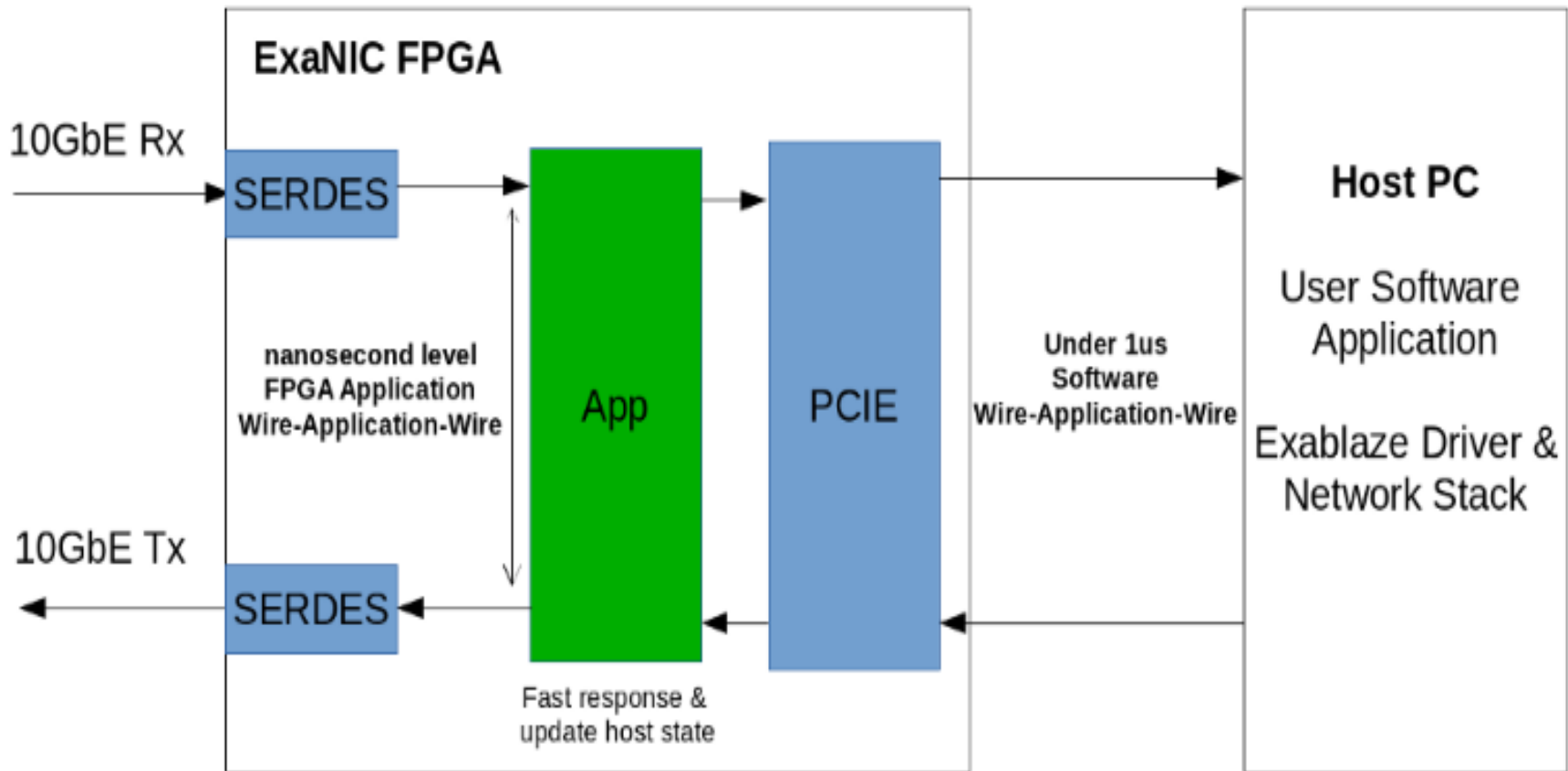


Vivado HLS





Trading on FPGA





FPGA Development Kit

✓ Interfaces:

All Ethernet Ports, DMA engines, user register space and user memory space.

✓ Supported Devices:

ExaNIC X10 featuring [Xilinx Kintex Ultrascale XCKU035](#)

ExaNIC X40 featuring [Xilinx Kintex Ultrascale XCKU035](#)

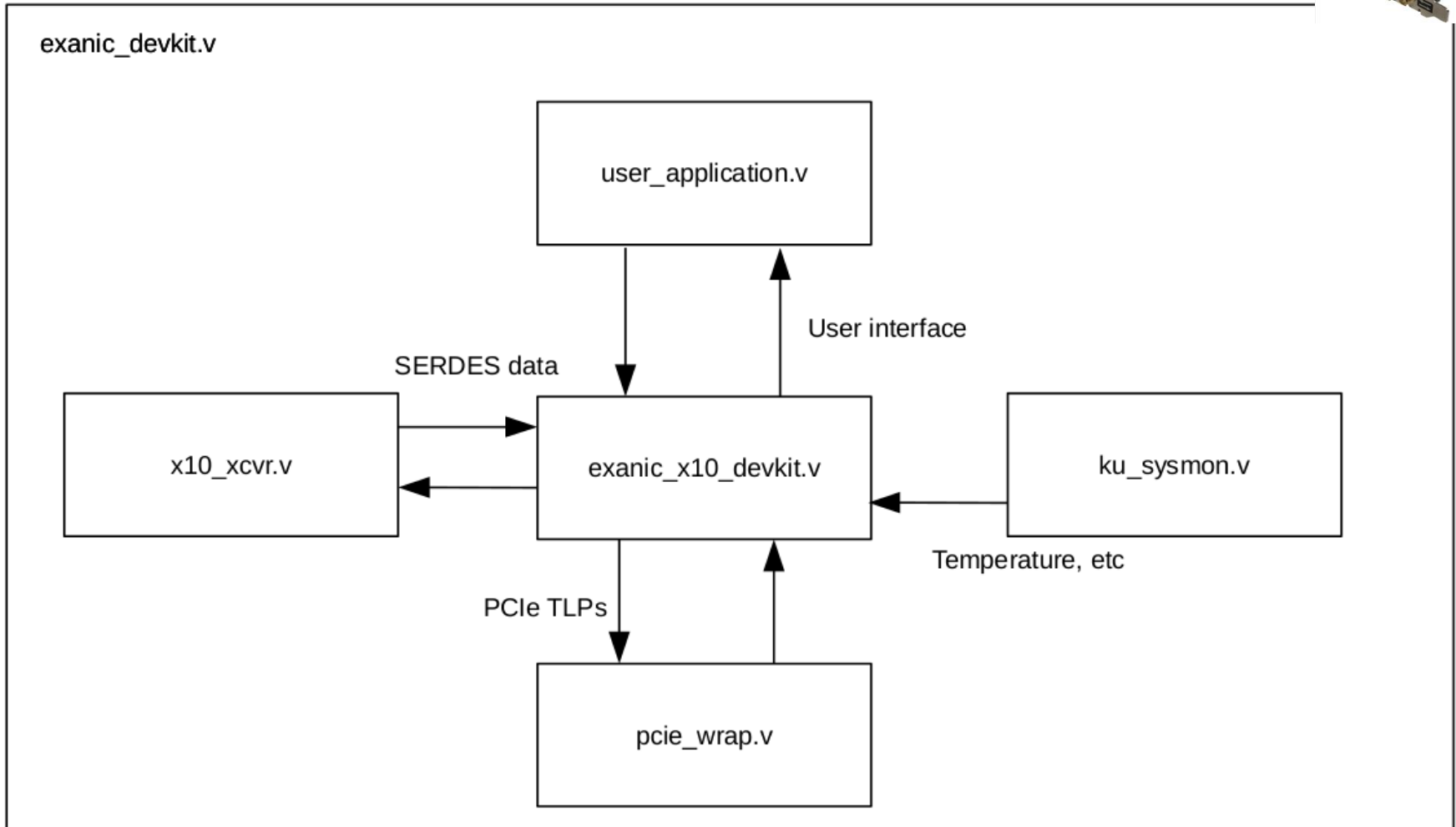
✓ Build process:

Makefile and build scripts included.

✓ Simulation and Verification:

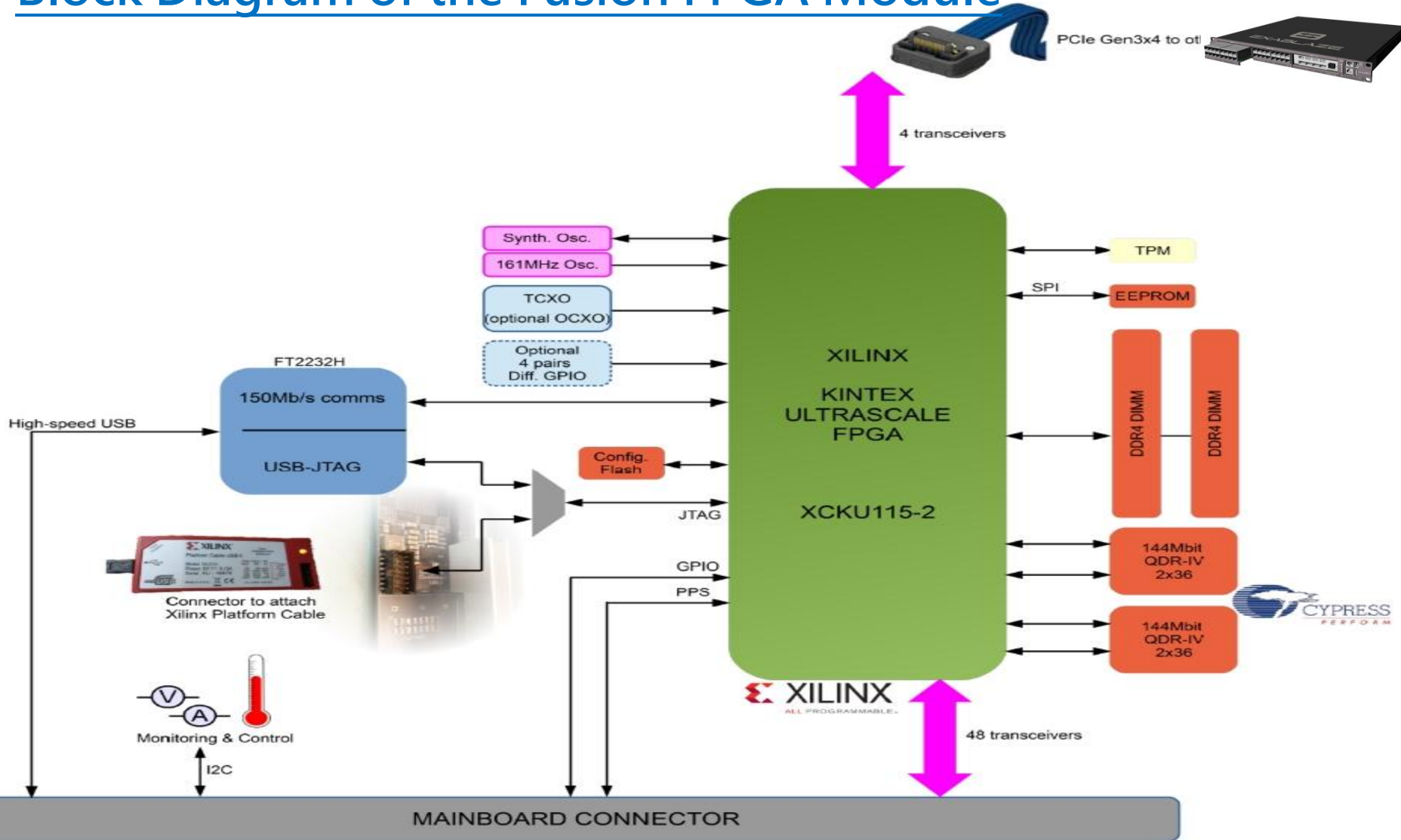
Full bus functional model allows simulation of all interfaces.

FDK Interfaces



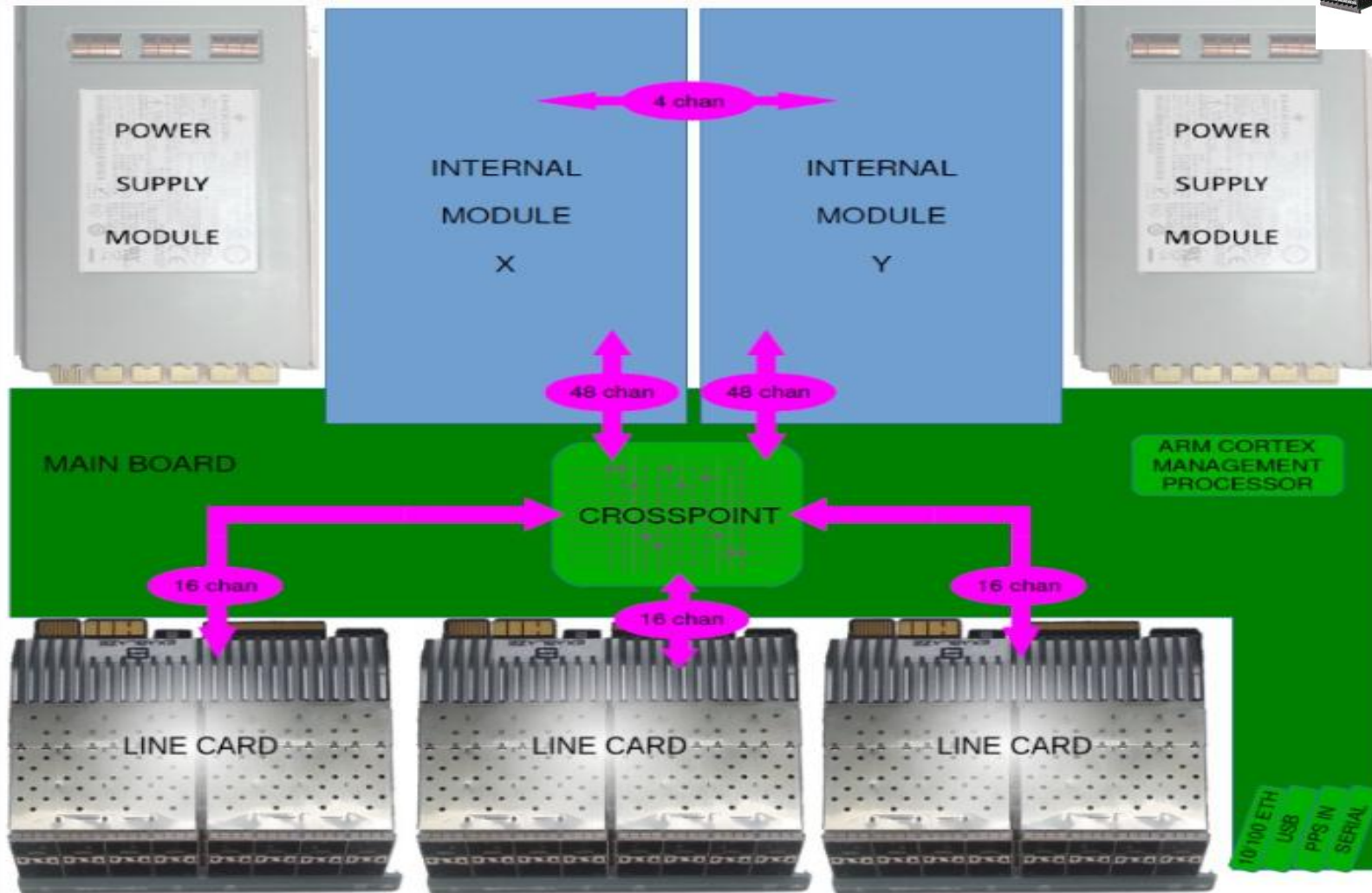
Block Diagram of the Fusion FPGA Module

ExaLINK



Connectivity of the Fusion FPGA Module

ExaLINK



Debugging with Vivado

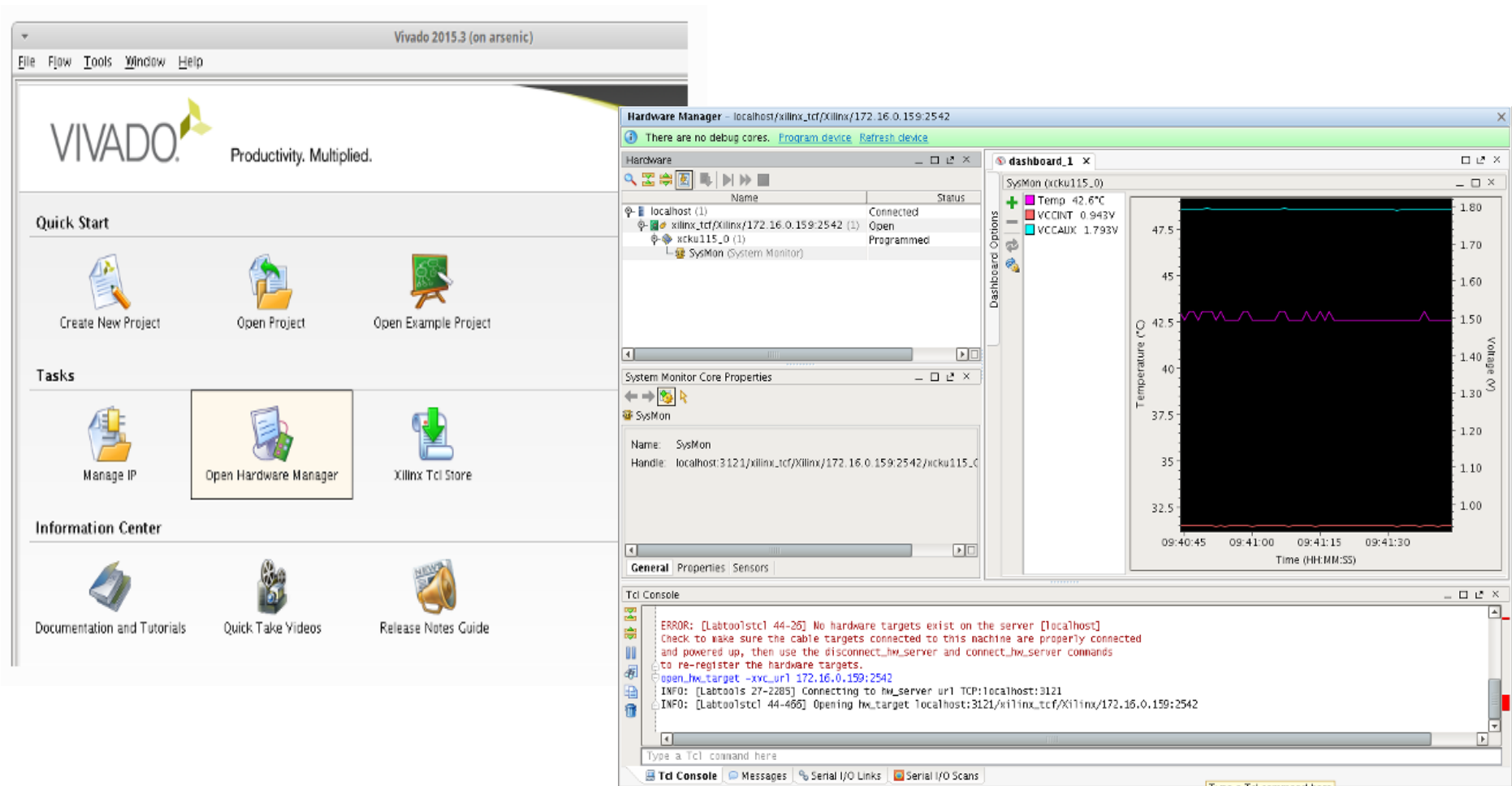
ExaLINK



Vivado connecting to the Fusion

Vivado HW Manager & SysMon Dashboard

ExaLINK



The screenshot displays the Vivado 2015.3 interface with the Hardware Manager and SysMon Dashboard windows open.

Hardware Manager (localhost/xilinx_tcf/Xilinx/172.16.0.159:2542)

Name	Status
localhost (1)	Connected
xilinx_tcf/Xilinx/172.16.0.159:2542 (1)	Open
xcku115_0 (1)	Programmed
SysMon (System Monitor)	

System Monitor Core Properties

Name: SysMon
Handle: localhost:3121/xilinx_tcf/Xilinx/172.16.0.159:2542/xcku115_0

Dashboard Options

- Temp: 42.6°C
- VCCINT: 0.943V
- VCCAUX: 1.793V

Graph Data:

Time (HH:MM:SS)	Temperature (°C)	VCCINT (V)	VCCAUX (V)
09:40:45	42.6	0.943	1.793
09:41:00	42.6	0.943	1.793
09:41:15	42.6	0.943	1.793
09:41:30	42.6	0.943	1.793

Tcl Console

```
ERROR: [Labtoolstcl 44-26] No hardware targets exist on the server [localhost]
Check to make sure the cable targets connected to this machine are properly connected
and powered up, then use the disconnect_hw_server and connect_hw_server commands
to re-register the hardware targets.
open_hw_target -xvc_url 172.16.0.159:2542
INFO: [Labtools 27-2285] Connecting to hw_server url TCP:localhost:3121
INFO: [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Xilinx/172.16.0.159:2542
```

THANK YOU !